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THRESHOLD ELEMENT CIRCUIT MECHANIZATIONS: AN ANNOTATED BIBLIOGRAPHY

SPECIAL BIBLIOGRAPHY
SB-62-57

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Compiled by:
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Lockheed

MISSILES & SPACE COMPANY

A GROUP DIVISION OF LOCKHEED AIRCRAFT CORPORATION

SUNNYVALE, CALIFORNIA

ABSTRACT

A bibliography has been prepared from recent (1960 to date) literature on computer threshold switching circuits and their components. Threshold switching devices are designed to perform logical switching functions. One class of switching functions, majority logic functions, has been emphasized in the bibliography. Entries are alphabetically arranged by senior personal author. A subject index is included.

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INTRODUCTION

A bibliography has been prepared from the recent (1960 to date) literature on computer threshold switching circuits and their components. Threshold switching devices are designed to perform logical switching functions based on two or more binary inputs. A two-input threshold element provides simple AND-OR switching. With three or more variable inputs, a wide variety of switching functions is possible. One such class of functions has been emphasized in the bibliography, namely, majority logic functions wherein the threshold element leads to a switching decision at the output based on the majority of signals introduced into the circuit, say two out of three, for a single 3-input majority element.

The compiler hopes this accumulation of data will illustrate some of the semantic illogic inherent in authors' usage of coined phrases to describe identical terms and relationships. For example, majority logic has been designated variously as voting logic, multilevel logic, linear input logic, linearly separable logic, threshold logic, and variable threshold logic. An obvious need exists for standardization, redefinition, and synthesis of existing switching circuit literature.

Entries in the bibliography are alphabetically arranged by senior personal author. A subject index is provided. The resources of the Lockheed Missiles and Space Company Technical Information Center were utilized in the preparation of the bibliography.

1. Akers, S. B.
On the algebraic manipulation of majority logic.
IRE TRANS. ELECTRONIC COMPUTERS
v. EC-10, p. 779, Dec 1961.

One of the difficulties which arises in manipulating algebraic expressions involving majority logic is the fact that ternary operations are involved. In this letter a method is outlined whereby this difficulty may be avoided.

2. Amarel, S., Cooke, G. and Winder, R. O.
MAJORITY GATE NETWORKS. Scientific
rept. no. 5. David Sarnoff Research Center,
Princeton, N. J. Rept. no. AFCRL-793, 24 Aug 61,
30p. (Contract AF 19(604)8423) ASTIA AD-268 907.

The problem of majority gate networks is discussed. A majority network of order n has (2n - 1) inputs and produces an output (it fires) when n of its inputs are excited (are fired). The problem of constructing such a network from smaller majority gates arises because in a large number of cases the network is not physically realizable with a single (2n - 1) input gate; this is due to the limited signal resolution possible in a practical electronic device. Suppose someone were to develop an extensive body of logical design theory employing five-input majority gates; and suppose a very fast device were developed which acted also as a majority gate, but could accept only three inputs reliably. Clearly, then, an appropriate answer to the problem that we have posed previously might allow direct application of the new device in already familiar networks.

3. Amodei, S. and Kosonocky, W. F.
High-speed logic circuits using common-base
transistors and tunnel diodes. RCA REV. v. 22,
p. 669–684, Dec 1961.

A complete set of logic circuits for operation at speeds of 100 Mc/s or higher, employing the combination of common-base transistors and tunnel diodes, are described. Emphasis is placed on circuits that take maximum advantage of the logical features of both devices as a means of achieving simplicity even in the realisation of more complex logical functions. The paper discusses the operation of the circuits, gives results of experimental tests and outlines analytical methods and models for evaluating their performance. The logic circuits included are basic gates, inverters, complementary gates, registers and adders.

4. Axelrod, M. S., Farber, A. S., and Rosenheim, D. E.
Some new high-speed tunnel-diode logic circuits.
IBM J. RES. & DEV. v. 6, p. 158–169, Apr 1962.

Several high-speed tunnel diode logic circuits are presented which perform majority-type logic or majority-type logic with inversion, and make use of a multiphase sinusoidal power supply to obtain signal directivity. Laboratory results are presented which show operation of these circuits at a 125 Mc/s pulse repetition rate with 2 nsec delay per logical decision. The circuits have also been operated at 250 Mc/s. These circuits are compared with some tunnel diode logic circuits previously reported in the literature to reveal certain system advantages of the new circuits. One circuit described is termed the Balanced Inductor Logical Element (BILE) and consists of a pair of matched tunnel diodes in series with two inductors; results of analogue computer analysis of this circuit are given. Another circuit is the Balanced Line Logical Element (BLLE) which consists of a pair of matched tunnel diodes in series with two delay lines; results of an analysis of the IBM 7090 are given. A full serial binary adder is described which has operated successfully at a bit rate of 125 Mc/s. The delay per logical stage is 2 nsec, the carry is produced in 2 nsec and the sum is available in 4 nsec.

5. Becker, P. W.
Static design of transistor diode logic. IRE TRANS.
CIRCUIT THEORY v. CT-8, p. 461–467, Dec 1961.

Two techniques for static design of drift-tolerant transistor diode logic are described. Three kinds of drift-tolerant design criteria are discussed: worst case, statistical design, the multiple worst case. The criteria illustrate different ways in which the information from the specification sheets may be applied to the design inequalities. The form of the design inequalities is discussed. Substantial simplicity is obtained by giving the inequalities a determinant form. Two ways of solving the design inequalities are demonstrated. Both methods will give the results in terms of available resistor values. The λ_S-method will give the set of highest resistor values which satisfies the design inequalities. The useful region method will determine a family of curves, each curve corresponding to a possible load on the circuit. The region which is limited by a curve illustrates all solutions to the design problem. A diagram which illustrates all possible resistor combinations with which a NAND circuit can drive a given load is derived. The AND or OR load in question determines which member of the family of curves is applicable. The design of an iterative NOR circuit with minimum power dissipation is described.

6. Bergman, R. H.
Tunnel diode logic circuits. IRE TRANS. ELECTRONIC COMPUTERS v. EC-9, n. 4, p. 430–8,
Dec 1960.

Considerations of diode uniformity requirements, stability problems and power supply requirements have led to a monostable type of logical circuit. The switching properties of this circuit are analyzed and found to depend upon the negative resistance-capacitance time-constant of the unit. The basic function performed by the circuit is a thresholding operation from which a set of logical building blocks is derived. Compatible dynamic and bistable storage schemes are discussed. The effect of diode variations upon the logical gains and delays of the circuits is of major importance. These properties are tabulated for tunnel diodes with 5% tolerances on knee current and voltage. Experimental circuits using diodes with a time constant of 1.4 ns have given a nominal switching time of 7.5 ns.

7. Boswell, J. M.
Digital comparison by NOR logic. INSTR. &
CONTROL SYSTEMS v. 34, p. 62–63, Jan 1961.

Brief account, with logic charts and block diagrams, of comparator circuits, showing that only two NOR elements are required to make an inequality comparison of two bits and only four for an equality comparison.

8. Brain, A. E.
The simulation of neural elements by electrical
networks based on multi-aperture magnetic cores.
IRE PROC. v. 49, p. 49–52, Jan 1961.

The paper describes a magnetic device which will

1) Compare an input current level to a controllable threshold level, and
2) If the input current exceeds the threshold a standard output signal is provided;
3) The output signal may be used to increment or to decrement the level of an analog storage element;
4) The stored analog quantity can be sensed nondestructively.

The article describes the design and operating characteristics of a specific configuration. As the author indicates, much of the theoretical work on neural networks assumes the existence of basic building blocks which possess one or more of the above properties.

The article was criticized in a recent letter by Harmon and the criticism rebutted. The two letters provide a good example of the difficulties encountered when a word like "neuron," which has a relatively precise biological definition, is used to describe a variety of devices which the inventors hope will process information approximately like a neuron. The problem is often compounded by a lack of understanding, on the part of the biologist and the computer builder, of each other's motives. The biologist would like to know more about the biological neuron while the computer builder wants to know only that which will help him to improve his computers.

9. Brzozowski, J. A.
RELIABILITY OF TRIANGULAR SWITCHING NETWORKS WITH INTERMITTENT FAILURES.
Scientific rept. no. 2. David Sarnoff Research Center, Princeton, N. J. Rept. no. AFCRL-785, 14 Aug 61, 47p. ASTIA AD-266 113.

A study was made of the problem of reliability of combinational switching networks constructed from logical gates which are subject to intermittent failures. Because of malfunctioning of components, a gate may realize any one of several Boolean functions and the probabilities of these functions are used to describe the behavior of the gate. In many cases, depending on the probability distribution, a more reliable gate can be obtained by using n + 1 identical n-input gates in a triangular structure (the outputs of n gates feeding the (n + 1) 'st). The gates so improved can be used again in a triangular structure. The properties of such recursions are investigated in detail for gates with probability distributions over unate functions and it is shown that arbitrary reliability can be achieved for the class of simple threshold gates, under suitable conditions.

10. Buzzell, G., Nutting, W. and Wasserman, R.
Majority gate logic improves digital system reliability. IRE INTERNAT. CONVENTION RECORD v. 9, n. 2, p. 264–70, 1961.

A majority gate implements a 'two-out-of-three' majority decision but, unless the reliability of this gate is very high, the overall reliability of the system will be lower than that of a completely non-redundant system. The module described combines a variety of logical functions with the majority gate. The gate function is accompanied by the summation of a physical quantity, produced by pulses applied to the inputs which are summed. When the total sum exceeds a preselected threshold level, the device changes its state. By varying the threshold level a variety of logical functions are obtained. The proposed design, which utilizes the principle of parametric excitation, has yet to be incorporated in a computer.

11. Cameron, Scott H.
SELF ORGANIZING NETWORKS. Annual rept. Armour Research Foundation, Chicago, Ill., 15 Feb 61–14 Feb 62, 14 Feb 62, 15p.
(Contract Nonr-339200, Proj. NR 048-165)
ASTIA AD-273 536.

The initial phases of a program directed toward the realization of complex adaptive logical networks by optical means are described. The logical networks with which the research is concerned are comprised of threshold devices in various configurations. The general hypothesis which underlies the program is that networks of threshold devices can be designed which will be capable of useful application to pattern recognition problems of several types, provided that we can discover simple, inexpensive means for their manufacture. Still another notion which we accept is that effective solutions to such problems will be found not in terms of networks of fixed behavior, but in terms of networks whose parameters can be easily altered by suitable action principles or adaptive strategies. While the program has been aimed at problems of both a theoretical and hardware nature, the major effort during the initial phase has been directed at the realization of a simple optical device for adaptive pattern recognition.

12. Chow, C. K.
Boolean functions realizable with single threshold devices. IRE PROC. v. 49, p. 370–371, Jan 1961.

Letter presenting a different approach to the problem discussed in a letter of the same title by M. C. Paull and E. J. McCluskey, Ibid. v. 48, p. 1335–1337, Jul 1960.

13. Chow, C. K.
ON THE CHARACTERIZATION OF THRESHOLD FUNCTIONS. AIEE Proc., 2nd Annual Symp. on Switching Circuit Theory, Detroit, Mich., Oct 17–20, 1961, p. 34–38.

The use of threshold gates rather than the more conventional AND and OR gates for the realization of logical networks promises a significant savings in the number of components. In the notation of the present paper, a threshold gate is a component with n binary inputs $x_1, x_2, \ldots, x_n$ and one binary output; the output is unity if and only if the weighted sum of the inputs equals or exceeds a threshold, i.e., if and only if

$$\sum_{i=1}^{n} N_i x_i \geq N_0$$

where the N_i, $i = 1, \ldots,$ are the weights, N_0 is the threshold and the addition is algebraic (non-Boolean).

This paper considers a problem which has received a considerable amount of recent attention – that of characterizing the class of switching functions realizable with a single threshold element, the so-called linearly separable class. Most other approaches have dealt with the function expressed as a minimum sum of products or as a truth table, and the test and realization procedures have been in the frame-work of the solution of simultaneous inequalities. The contribution of the present paper is a new approach to the characterization problem which may lead to considerably simpler testing and realization methods.

Let F be a switching function and let $a_i(F)$ represent the number of times x_i is unity in the list of truth table points for which F is unity. The vector

$$a(F) = [a_1(F), a_2(F), \ldots, a_n(F)]$$

can be considered to be the vector sum, in the usual switching space, of all the vectors for which F is unity. Further let m(F) be the number of truth table points for which F is unity. The principal result of this paper is that a(F) and m(F) characterize F for the purpose of testing and realization as a single threshold gate; stated more precisely,

> Let F and G be functions of n variables. If m(F) = m(G) and a(F) = a(G), then either both F and G are realizable or both are not realizable. If F is realizable, then G = F.

Thus, there are n + 1 parameters which uniquely characterize the realizability of n variable functions. A test and realization procedure based on these parameters would presumably be much simpler than any that have been proposed thus far. However, except for a limited class of functions discussed in the paper, the problem of determining realizability from these parameters remains unsolved.

14. Chow, W. F.
Tunnel diode logic circuits. ELECTRONICS v. 33,
n. 26, p. 103–7, 24 Jun 1960.

The basic characteristic of a tunnel diode permits both monostable and bistable operation. Two forms of logic are available; the first is analogue-threshold in which the diode generates an output when the sum of the currents from a number of inputs is just great enough to trigger it. The second is majority decision logic, generating a positive or negative output as the majority of an odd number of inputs are positive or negative respectively. The main difficulty in using such circuits is their bilateral behavior and special means must be employed to ensure a flow of information in a predetermined direction. In this respect tunnel diode logic resembles parametron logic and similar solutions to the problem may be invoked. Equations are presented leading to sets of curves which relate the component and diode tolerances to the number of inputs and outputs allowable. A typical result requires 3% diode and 2% component tolerances for 3 inputs and 3 outputs.

15. Coates, C. L. and Lewis, P. M., II
Linearly separable switching functions.
J. FRANKLIN INST. v. 272, n. 5, p. 366–410,
Nov 1961.

A threshold switching element is a multi-input generalization of an "and" or "or" gate. Its output is unity if and only if the weighted sum of its inputs equals or exceeds a threshold: $\Sigma a_i x_i \geq T$; otherwise its output is zero. A linearly separable function is a switching function that can be realized with one such element. This paper studies

in some detail the properties of linearly separable functions. In terms of these properties a test and realization procedure is derived. The test consists of three parts which for every switching function provide either a realization or a proof that the function is not linearly separable. Not all parts are necessarily required for testing every function. A function of eight variables can be tested and realized in about thirty minutes of hand computations.

16. Cohn, M. and Lindaman, R.
Axiomatic majority-decision logic. IRE
TRANS. ON ELECTRONIC COMPUTERS
v. EC-10, p. 17–21; Mar 1961.

An algebra suited to logical design with majority-decision elements (parametrons, Esaki diodes, etc.) is developed axiomatically. The utility of the new algebra is demonstrated by resolving sample problems.

17. Couch, R. W., Rashid, A. F. and Spence, R.
A potential microwave computer element.
IRE PROC. v. 49, n. 8, p. 1338–9,
Aug 1961.

A two-state device can be made by having an oscillator with two stable frequencies. Such a device may consist of two tuned circuits in series with a nonlinear negative conductance such as a tunnel diode. An experimental model has been made from a doubly-resonant quarter-wave trough line with the diode connected across the ends of the two inner conductors, and stable oscillation frequencies of 250 Mc/s and 375 Mc/s obtained. Experiments on a lower frequency version (600 kc/s and 735 kc/s) indicate that a useful fan-out ratio may be obtained with a switching time of about 10 c/s, switching being achieved by superimposing the desired frequency, so that to obtain a switching time of 1 nsec characteristic frequencies of tens of kMc/s are needed. Logic operation can be on the majority principle; for example, AND and OR circuits are realized by injecting two input signals and a continuous frequency bias signal all of the same amplitude into a bistable oscillator.

18. Crane, Hewitt, D.
THE AXON AS A NEURISTOR; AN ANALYSIS
OF NERVE TRANSMISSION. Stanford Research
Inst., Menlo Park, Calif. Mar 61, 38p.
(Contracts AF 33(616)7567 and Nonr-321200)
(WADD TN 61-26) ASTIA AD-254 379.

Neuristor is the name assigned to the class of devices that exhibits attenuationless signal propagation, as in the attenuationless propagation of a burning zone along a simple chemical fuse, or the attenuationless propagation of an electrical discharge

along the axon of a nerve fiber. Early studies have shown that totally distributed electronic lines can be realized that exhibit similar propagation properties; furthermore, many different types of lines can be realized, each characterized by different forms of mathematical systems. An analysis of nerve transmission yields excellent electrical models and equation forms. A result was the realization that the propagation along the axon of a nerve fiber, and that along a (conceptually) rechargeable fuse appear to be fundamentally different, although their terminal properties are identical. Lines realized according to the former style are referred to as N (for nerve) type lines, and those realized according to the latter style as F (for fuse) type lines. The difference between the two forms of line is made clear by example; relay lines built according to both forms are indicated.

19. Crane, H. D.
The neuristor. IRE TRANS. ON ELECTRONIC COMPUTERS v. EC-9, p. 370–371, Sep 1960.

The properties of a novel universal logic and memory device, called a neuristor because of its similarity of operation to that of an ionic neuron, are described. The basic requirements for the device are, 1) a distributed energy source, 2) distributed energy storage and, 3) a distributed active device. Attenuationless discharge signals are propagated as uniform velocity pulses. After propagating a signal, each portion of the device has a refractory period. A bit is stored as a pulse in a closed loop. Logic is performed by the annihilation of pulses upon collision. An example of a neuristor is a strip of thermistor material in parallel with an equal length of distributed capacitor, the combination being energized by a distributed current source.

20. Crane, H. D.
ON THE COMPLETE LOGIC CAPABILITY AND REALIZABILITY OF TRIGGER-COUPLED NEURISTORS. Stanford Research Inst., Menlo Park, Calif. Interim rept. no. 4, Jul 61, 65p.
(Contracts Nonr-321200 and AF 33(616)7567)
ASTIA AD-262 198.

Neuristors may be interconnected in two basically different modes, defined as T junctions and R junctions; T for triggering and R for refractory. Study was performed to determine whether complete logic capability may be achieved with neuristor junctions that are based only on trigger-coupling. Study was motivated by the concern that R junctions may be somewhat more difficult to realize physically than T junctions. To achieve complete logic, it must be possible to synthesize with a triggering type of connection the basic inhibition property so directly offered by the R junction. Two techniques for achieving this type of connection are outlined. It is indicated that, based on these techniques, trigger-connected junctions can be realized which offer full logic capability.

21. Dadda, L.
The synthesis of switching networks made up of threshold circuits. ALTA FREQUENZA v. 30, n. 2, p. 127–34, Feb 1961. (In Italian).

Only certain classes of switching functions are realizable with a single threshold circuit element. Procedures are described for achieving other functions by the use of two or more such elements. Results are tabulated for functions of two or three independent variables, and procedures to follow for the case of four or more variables are given.

22. Dadda, L.
Synthesis of threshold logic combinatorial networks. ALTA FREQUENZA v. 30, p. 224–231, Mar 1961. (In Italian)

The problem of synthesizing arbitrarily assigned switching functions using only threshold elements is considered. Elementary threshold functions, i.e., functions that can be implemented by a single threshold circuit, are first characterized for the cases of 2, 3, and 4 variables. Two methods are then illustrated for the synthesis of non-elementary functions, and the results for the primitive functions of the symmetry classes of 2 and 3 variables are given.

23. Dadda, L.
On the synthesis of switching networks with the least number of components. ALTA FREQUENZA v. 30, n. 4, p. 272–8, Apr 1961. (In Italian)

Known methods for the synthesis of switching functions consider only the case of expressions of "logical sum of logical products." A procedure, which is a generalization of existing procedures, is then explained which permits the synthesis of other types of expression, especially those of "logical sum of arbitrarily assigned elementary functions." The method is particularly suitable for programming a computer.

24. Dumaire, M.
The symmag (a high-speed static magnetic switching element). BULL. SOC. FRANC. ELECT. (SER. 8) v. 1, n. 10, p. 703–10, Oct 1960. (In French)

The basic Symmag element has two separate identical square-loop ferrite cores, each with four windings, input, output, excitation and bias. Both excitation and bias windings are series-connected between cores. A permanent and d.c. bias sets each core in positive saturation and an a.c. signal is supplied to the excitation winding. A positive input to one core keeps it in saturation during excitation while the other swings giving an output. Diodes in the output windings ensure unidirectional outputs and so an input 1 or 0 to one core results in an amplified 1 or 0 output from the other core. The complementary nature of input to output between cores results in a simultaneous presentation of "and" and "or" operations. Two practical basic elements are described and the realization of other operations by interconnection of them is discussed. The element has been developed for excitation frequency ranges of 40-700 kc/s. An output discrimination between 1 and 0 better than 50 to 1 and high insensitivity to excitation variation is achieved.

25. Einhorn, S. N.
The use of the simplex algorithm in the mechanization of Boolean switching functions by means of magnetic cores. IRE TRANS. ELECTRONIC COMPUTERS v. EC-10, n. 4, p. 615–22, Dec 1961.

An algorithm is presented for mechanizing Boolean switching functions by means of a net of magnetic toroidal cores. The algorithm is referred to as Simplex and is programmed for a digital computer. Computer solutions specify the wiring configuration for a core or net of cores yielding a device for performing combinational logic. Switching functions are realizable in essentially one clock time. The logical designer may synthesize a function directly from the truth table without proceeding in the customary manner of expressing the function in Boolean canonical form and then attempting to minimize with respect to hardware or other criteria by means of algebraic manipulation or a mapping or charting technique.

26. Fischler, M. A.
A PROPERTY OF UNATE SWITCHING FUNCTIONS WITH AN APPLICATION TO LOGICAL DESIGN. Lockheed Aircraft Corp., Sunnyvale, Calif. Technical rept. on mathematics. Rept. no. 6-90-61-5, May 60, 13p. ASTIA AD-257 869.

27. Fischler, M. A. and Poe, E. A.
Threshold realization of arithmetic circuits. IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, v. EC-11, n. 2, p. 287–288, Apr 1962.

Brief note describes loop-free combinational threshold circuits which were designed using a synthesis technique still under development at Lockheed Missiles & Space Co., Palo Alto, Calif.

28. Foote, R. S. and Harrison, W. V.
High-speed switching circuitry using tunnel diodes. IRE TRANS. CIRCUIT THEORY v. CT-8, p. 468–473, Dec 1961.

A discussion of various techniques which may be used in obtaining high speed digital circuit operation is presented. To gain these advanced digital speeds, tunnel diodes have been incorporated into transistor circuitry. The fast rate of change of voltage and the bistable capabilities of the tunnel diode are the characteristics which provide for higher speeds. Development has been mainly applied to the application of the GaAs tunnel diode in circuitry because of the higher output voltage available. Some of the ultimate speeds attainable in circuits providing impedance transformation and amplification are discussed, followed by circuit applications in more detail.

29. Gabelman, Irving Jacob
THE FUNCTIONAL BEHAVIOR OF MAJORITY (THRESHOLD) ELEMENTS. Syracuse University (Ph. D. thesis) 1961, 117p.

A majority or threshold element is a device with a finite number of inputs and a single output. The output, Fn, is a Boolean function of the n binary valued variables $(x_1, x_2, \cdots, x_n)$ **applied to the inputs. An investigation into the functional behavior and logical properties of this device is the subject of this dissertation. The three principal topics of the investigation are analysis, realizability and synthesis.**

The analysis of a threshold element is the determination of the output Boolean function, Fn, when the input variables and their multiplicities are specified. The multiplicity of an input variable x_i **is the number of inputs to which the variable is applied. The fundamental problem in analysis is the determination of** F_n **when the number of inputs is nominally large.**

An algorithm is given which permits a simple straight-forward determination of F_n **in reduced, disjunctive form. Since variables with equal multiplicities appear symmetrically in** F_n**, a simplification of the form and complexity of** F_n **may be obtained by expressing it as the product of symmetric functions. An alternative analysis technique using a "Tree of Compositions" is also given.**

While a large number of Boolean functions may be realized as the output of a single threshold element, not all functions are so realizable. Those F_n **which are, are said to belong to the class R.**

The objective in a study of realizability is the establishment of necessary and sufficient conditions for $F_n \epsilon R$. It is shown that a necessary but not sufficient condition for $F_n \epsilon R$ is that F_n be unate; i.e., that any variable appearing in F_n must be complemented or uncomplemented but not both.

The question of realizability is considered from a geometrical viewpoint by associating with F_n, a subset S_n of the vertices of the unit n cube. It is shown that if $F_n \epsilon R$, then the associated subset S_n must be strictly separable by an (n - 1) hyperplane from the remaining vertices of the unit n cube, the subset $\bar{S}_n$.

A theorem from the mathematics of convex sets gives the necessary and sufficient conditions for the separation of S_n and $\bar{S}_n$; however, these are difficult to apply. A simplification of these conditions is required. Various simplification conjectures which have appeared in the literature are examined. A new conjecture is advanced – that for all $n < 9$, if $F_n \notin R$, then some edge of the convex hull of S_n must intersect an edge of the convex hull of $\bar{S}_n$. This intersection of edges is termed a $\Sigma 2$ condition. A method is given which allows for a simple determination of the existence of the $\Sigma 2$ condition.

Synthesis is the specification of the element configuration required to realize a given Boolean function. There is associated with F_n, a set of 2^n inequalities obtained from the 2^n possible valuations on the n Boolean variables applied to the inputs. The solution of these inequalities yields the values of the m_i; i.e., establishes the desired configuration. Two synthesis procedures, both based on solving these inequalities, are given.

No easily applicable criteria have been formulated which allow for a determination of whether a given F_n belongs to the class R. If, however, it is known that $F_n \epsilon R$, then certain transformations can be effected on F_n which result in a realizable function F_p. There do exist, in addition, observable properties of the form of F_n which can be used for this determination and also in many instances a simple synthesis. Permissible transformations and these observable properties are examined.

30. Gabelman, I. J.
A note on the realization of Boolean functions using a single threshold element. IRE PROC. v. 50, p. 225–226, Feb 1962.

Letter in which it is shown that a theorem contained in the mathematics of convex sets supplies the necessary and sufficient conditions for the class of Boolean functions capable of being realized as the output of a single threshold element.

30a. Goto, Eiichi
Threshold, majority and bilateral switching devices. Paper presented at a SYMPOSIUM ON THE APPLICATION OF SWITCHING THEORY IN SPACE TECHNOLOGY, 27 AND 28 FEB AND 1 MAR 1962 AT SUNNYVALE, CALIF. PROCEEDINGS to be published by Stanford University Press, 1963.

The two main stimulating factors leading to increased activity in the threshold or majority logic field are (1) the development of a class of practical computer components, such as parametrons, magnetic core switches and Esaki diode circuits, which all operate on the mathematical principle of linear summation and threshold logic decision and (2) its potential application to neuron-like or adaptive systems. The author believes there are two approaches in threshold logic, the idealistic and the practical or realistic. Both are necessary for full development of the art. Sections cover the author's method for classifying Boolean functions (called self-dual classification) and properties of weights, threshold and the number of linear input functions. Proofs are provided in appendices. Goto illustrates the close relationship between the systematic use of redundancy in threshold logic and the use of error-correcting codes or load sharing schemes in address selection.

31. Hamann, Robert Arthur
APPLICATION OF P-N-P-N DIODES TO MAJORITY LOGIC CIRCUITS. Air Force Inst. of Tech., Wright-Patterson Air Force Base, Ohio. Rept. no. GE/EE/61-5 (master's thesis) Aug 61, 48p. ASTIA AD-269 417.

The static characteristics of a two-terminal P-N-P-N diode are discussed. Switching of this diode is controlled by varying the applied voltage and current. Majority logic is then considered. Functions can be converted to majority form from Boolean expressions using an axiomatic majority-decision logic; majority logic circuits can be analyzed with Karnaugh maps. A three-input majority logic circuit using P-N-P-N diodes and passive circuit elements is presented. An analysis of the circuit shows that it is possible to obtain any number of outputs with component tolerances of 5%. The operating frequency is less than 200 kc. The circuit is practical for application where high speed is not required and diodes can be obtained at a low cost.

32. Henderson, K. W.
A CATALOG OF LINEARLY SEPARABLE FUNCTIONS OF TWO TO FIVE VARIABLES. Lockheed Aircraft Corp., Sunnyvale, Calif. Rept. no. LMSD-288176, Feb 60.

Considerable interest has arisen recently in the properties of linearly separable truth functions, because of the possibility of constructing simple neuron-like circuit elements based on these properties. It appears that such circuit elements might lead to simpler digital circuitry for some applications. Such circuitry would include so-called self-organizing or self-adaptive networks, and ultimately, it is hoped, extremely versatile pattern recognition devices. It is also believed that such circuit elements might be useful in neurophysiological studies involving simulation of neurons, either individually or in networks.

This report presents a catalog of sets of weights and thresholds for all the possible types of linearly separable functions of two to five variables. A few fragments of information, probably not previously known, have come from this study in addition to the catalog data. Some of this information is of an empirical nature and lacks mathematical proof. Novertheless, the catalog has numerous useful purposes, and it is hoped that its publication will spur further interest among engineers and mathematicians.

33. Highleyman, W. H.
LINEAR DECISION FUNCTIONS, WITH APPLICATION TO PATTERN RECOGNITION. IRE PROC. v. 50, p. 1501–9, Jun 1962.

Many pattern recognition machines may be considered to consist of two principal parts, a receptor and a categorizer. The receptor makes certain measurements on the unknown pattern to be recognized; the categorizer determines from these measurements the particular allowable pattern class to which the unknown pattern belongs. This paper is concerned with the study of a particular class of categorizers, the linear decision function. The optimum linear decision function is the best linear approximation to the optimum decision function in the following sense:

1) "Optimum" is taken to mean minimum loss (which includes minimum error systems).
2) "linear" is taken to mean that each pair of pattern classes is separated by one and only one hyperplane in the measurement space.

This class of categorizers is of practical interest for two reasons:

1) It can be empirically designed without making any assumptions whatsoever about either the distribution of the receptor measurements or the a priori probabilities of occurrence of the pattern classes, providing an appropriate pattern source is available.

2) Its implementation is quite simple and inexpensive.

Various properties of linear decision functions are discussed. One such property is that a linear decision function is guaranteed to perform at least as well as a minimum distance categorizer. Procedures are then developed for the estimation (or design) of the optimum linear decision function based upon an appropriate sampling from the pattern classes to be categorized. Finally, the concepts and procedures thus developed are applied for illustrative purposes to the recognition of hand-printed numbers.

34. Holst, P. A.
Bibliography on switching circuits and logical algebra. IRE TRANS. ELECTRONIC COMPUTERS v. EC-10, p. 638–661, Dec 1961.

This bibliography, which covers material published from 1893 to 1958, contains nearly 700 references to articles, books, seminars and other bibliographies pertaining to the theory of switching circuits and logical algebra. A relatively large number of references are to foreign works, of which the Russian contribution is by far the greatest. Appended to the chronological bibliography are a list of books, a list of other bibliographies, an author index, a (fairly broad) subject index, a list of periodicals, and a list of frequently used Russian abbreviations.

35. Hu, Sze-Tsen
MAXIMAL POINTS OF A REGULAR TRUTH FUNCTION. Lockheed Aircraft Corp., Sunnyvale, Calif. Technical rept. on mathematics. Rept. no. 6-90-61-13, Jun 1961, 27p. ASTIA AD-262 918.

Every canonical linearly separable truth function is a regular function, but not every regular truth function is linearly separable. The most promising method of determining which of the regular truth functions are linearly separable requires finding their maximal and minimal points. In this report is developed a quick, systematic method of finding the maximal points of any regular truth function in terms of its arithmetic invariants.

36. Hu, Sze-Tsen
ON THE CLASSIFICATION OF LINEARLY SEPARABLE TRUTH FUNCTIONS. Lockheed Aircraft Corp., Sunnyvale, Calif. Technical rept. on mathematics. Rept. no. 6-90-61-26, Jan 1961, 17p. ASTIA AD-263 823.

A solution to the classification problem of the linearly separable truth functions of n variables by reducing it to the enumeration of a special kind of truth functions called canonical truth functions is given. The classification problem is formulated and the canonical truth functions are defined. The key lemma is proved, and the reduction is described.

36a. Hurley, Richard B.
Quantized probability design. ELECTRONIC EQUIPMENT ENGINEERING p. 51–54, Sept 1961; p. 65–68, Oct 1961.

A technique for designing transistor logic circuits based on statistical probability is described. A set of quantized rules is used for the actual design and statistical methods are used only for checking.

37. Kaenel, R. A.
Hysteresis-free tunnel-diode amplitude comparator. IRE TRANSACTIONS ON ELECTRONIC COMPUTERS v. EC-11, n. 2, p. 286–287, Apr 1962.

Circuit described performs the comparator function at a high switching speed typical of tunnel diodes and exhibits a high degree of thermal stability.

38. Kautz, W. H.
AUTOMATIC FAULT DETECTION IN COMBINATIONAL SWITCHING NETWORKS. Stanford Research Inst. Apr. 1961, 48p. ASTIA AD-267 005.

A study has been made of the logical design of economical combinational switching networks which contain sufficient redundancy so that the presence of any single fault can be detected. Within broad limits any isolated fault in a single-output network

may be detected with about 2:1 redundancy, through duplication of the irredundant network and the addition of a comparator gate. A reduction of the redundancy ratio below 2:1 is shown to be usually possible. Branch-type networks, e.g., those made up of relay contacts or cryotrons instead of gate-type elements, are also considered. If the designer is free to use some non-branch-type elements in the detection circuitry, the same low redundancy ratios achievable in gate-type circuitry can be obtained. Finally, several examples in applications areas of importance in conventional digital systems are discussed, including some comparators, calculating networks, code converters and decoding trees.

39. Kautz, W. H.
The realization of symmetric switching functions with linear-input logical elements.
IRE TRANS. ON ELECTRONIC COMPUTERS
v. EC-10, p. 371–378, Sep 1961.

The problem of synthesizing switching networks out of linear-input (threshold) elements for the class of symmetric switching functions is studied. Tight bounds are derived for the number of elements required in a minimal realization, and a method of synthesis is presented which yields economical networks. Minimal networks result for all symmetric functions of no more than about twelve variables, and for several other cases. In particular, it is shown how the parity function of any number n of variables can be realized with about $\log_2$ (n) elements.

40. Kilmer, William
ITERATIVE SWITCHING NETWORKS COMPOSED OF COMBINATIONAL CELLS. Scientific rept. no. 1. Montana State Coll., Bozeman.
Rept. no. AFCRL TN 60-1108, 1 Dec 1960, 41p.
(Contract AF 19(604)6619) ASTIA AD-253 612.

An n-dimensional iterative switching network consists of a number of identical logic cells uniformly interconnected through discrete information channels along each of n axis directions in space. This paper antecedes a general treatment of such networks by focusing on the 1-dimensional case, or the case of a linear cellular array, where cells are combinational, the information channels between them are bilateral, and switching is done synchronously with unit delay through each cell. These constraints are justified by demonstrating the behavioral equivalences which exist between corresponding combinational-cell and sequential-cell networks. Three classes of networks are formed according to whether or not information flowing in one direction along the cellular array is dependent upon that flowing in the other direction. A synoptic discussion of Hennie's steady-state analysis results is given for the three classes, and the relative merit and character of the class having mutually dependent information flow

is discussed. The main part of the paper deals with this class as the only one which can exhibit stable-state memory properties, and proves several important theorems concerning these properties. A transposition of some of Hennie's previous results is given as a start on the transients and cycling problems.

41. Kogan, I. M.
The stability of waiting threshold devices with spread of the parameters. RADIOTEKHNIKA v. 15, n. 11, p. 65–72, Nov 1960. (In Russian)

An approximate "threshold stability function" is introduced, and enables the probability of a point representing a parameter of the device falling into the domain of the parameter space lying below the threshold surface. Thus geometrical constructions can be used to find the probability. By using the above threshold function, a spread of the parameters can lead to substantial lowering of the stability of this device.

42. Lade, R. W.
Directly coupled tunnel diode-transistor logic.
SOLID STATE DESIGN v. 3, p. 43–48, Jan 1962.

The basic tunnel diode-transistor logic (TDTL) circuit and an extension of the basic circuit wherein the need for threshold gating is eliminated are discussed. The basic directly-coupled TDTL gating connection is analyzed and typical circuits performing OR and AND logic are described. Switching speeds are determined almost entirely by the switching speed of the tunnel diode employed. Isolation is provided by the current gain figure of the transistor, thus permitting unusually high fan-in and fan-out to be achieved. Typical experimental circuits and results are presented. An important advantage of the circuit is that a nonthreshold technique for gating is achieved which permits parameter tolerances to be less stringent than in a comparable tunnel diode design.

43. Ledley, R. S., Boyle, D. R. and Wilson, J. B.
COLLECTED PAPERS ON SWITCHING CIRCUIT THEORY AND LOGICAL AND SYSTEMS DESIGN.
National Biomedical Research Foundation. Oct 1961, 36p. ASTIA AD-266 580.

Boolean matrices applied to sequential circuit theory and threshold logics; Multivalued logic devices for simulating threshold neurons; Organization of large memory systems; An algorithm for rapid binary division.

44. Lindaman, R.
A theorem for deriving majority-logic networks within an augmented Boolean algebra. IRE TRANS. ON ELECTRONIC COMPUTERS v. EC-9, p. 338–342, Sep 1960.

Recent developments in computer technology have produced devices (parametrons, Esaki diodes) that act logically as binary majority-decision elements. Conventional design techniques fail to utilize fully the logical properties of these devices. The resulting designs are extravagant with respect to the number of components used and the operating time required. This paper reviews the conventional technique briefly and proposes an alternative method that produces more nearly minimal designs.

45. Mattson, R. L.
AN APPROACH TO PATTERN RECOGNITION USING LINEAR THRESHOLD DEVICES.
Lockheed Aircraft Corp., Missiles & Space Div. Rept. no. LMSD 702 680, Sep 1960.
ASTIA AD-246 244.

The general problem of pattern recognition is represented as a mapping between three fundamental spaces: a pattern space consisting of the patterns of interest, a data space consisting of measurements made on the patterns, and a classification space consisting of the various classes of patterns to be recognized. The mapping from pattern space to data space is accomplished by equipment which measures characteristics of the patterns of interest which have utility for the system. Three examples are presented to illustrate the way in which this initial processing might be accomplished. An automatic design procedure is presented for a binary classification system capable of mapping from the data space into a recognition class in the classification space. The binary classification system uses networks of linear threshold devices to perform this mapping. These networks are easily designed by a high-speed digital computer, and the time and storage requirements are small enough to make the procedure attractive for a wide variety of pattern recognition problems. The networks can be constructed by using magnetic core materials, or simulated by using a special-purpose digital computer. If the initial data processing of the patterns of interest isolates a set of characteristics which can be effectively used, the rest of the pattern recognition problem becomes fully automatic.

46. Mayeda, Wataru
SYNTHESIS OF THRESHOLD NETWORKS BY ALOGIC FUNCTIONS. Coordinated Science Lab., U. of Illinois, Urbana. Rept. no. R-124, Mar 61, 27p. (Contract DA 36-039-sc-85122) ASTIA AD-254 128.

By the use of functions called alogic functions consisting of logic operations as well as algebraic operations, the synthesis of threshold or majority networks becomes simple especially for the realization of a switching function by a single threshold or a single majority element. The first section introduces a particular threshold element called a W-element and shows that W-elements and scalar multipliers are sufficient to represent any threshold or majority networks. The second section shows the properties of alogic functions and clarifies that the synthesis of threshold or majority networks is equivalent, to obtain a suitable alogic function from a switching function. The third section gives a rather simple method for the realization of a switching function by a single threshold or a single majority element. The extension of applications of alogic functions to synthesis of sequential circuits is promising.

47. McIsaac, P. R. and Itzkan, I.
A new class of switching devices and logic elements. IRE PROC. v. 48, p. 1264–1271, Jul 1960.

This paper describes a new class of devices that perform switching and logic at microwave frequencies and employ electron beams and circuit elements closely related to those used in modern microwave tube technique. A preliminary device demonstrating the ability of a microwave signal to control a direct current is described, as is also an experimental travelling-wave interaction type tube which demonstrates the ability of one microwave signal to control another.

48. McNaughton, R. M.
Unate truth functions. IRE TRANS. ON ELECTRONIC COMPUTERS v. EC-10, p. 1–6, Mar 1961.

Some applications of an elementary study of unate truth functions are discussed. One application is a method of deciding when a truth function is linearly separated, i.e., is expressible as a linear polynomial inequality in its arguments (letting 1 represent truth and 0 represent falsity). Other applications are to contact nets and to rectifier nets.

49. Miller, H. S.
Majority gates applied to simultaneous comparators.
IRE TRANS. ELECTRONIC COMPUTERS v. EC-10,
p. 94–95, Mar 1961.

This letter points out an application of majority gates to a simultaneous comparator net. By "simultaneous", it is inferred that simultaneous answers to the questions Is X > Y?; Is X = Y?; and Is X < Y? will appear at the output of the net.

50. Miller, H. S. and Winder, R. O.
MAJORITY LOGIC BY GEOMETRIC METHODS.
Scientific rept. no. 4. David Sarnoff
Research Center, Princeton, N. J. Rept. no.
AFCRL-792, 13 Jul 61, 6p. (Contract
AF 19(604)8423) ASTIA AD-268 906.

The usefulness of a geometric approach to the following problem is presented: Given an n-argument switching function and i-input majority gates as building blocks, devise a network which represents the given function. This problem has been treated algebraically. Two-level realizations will be derived, and problems with larger values of n and i are considered. In these cases, multi-level realizations must be permitted. The synthesis procedures described employ geometric intuition (namely, matching known patterns with given patterns), and do not guarantee optimal solutions.

51. Miller, H. S. and Winder, R. O.
Majority-logic synthesis by geometric methods.
IRE TRANSACTIONS ON ELECTRONIC COMPUTERS v. EC-11, n. 1, p. 89–90, Feb 1962.

Geometric approach to problem: Given an n-argument switching function and i-input majority gates as building blocks, devise a network which represents the given function.

52. Minnick, R. C.
Linear-Input logic. IRE TRANS. ON ELECTRONIC COMPUTERS v. EC-10, p. 6–16,
Mar 1961.

Techniques for the logical design of magnetic core circuits to produce arbitrary single-output combinational switching functions are developed. The approach is based on the relationship of a single magnetic core circuit to a linearly separable switching function. A synthesis procedure which uses a pair of logical primitives, AND with NOT and OR with NOT, which are similar to the STROKE primitive and its inverse, is developed. Procedures for the synthesis of symmetric functions which require no more than the integral part of $(n + 3)/2$ cores, approximately half the number used in previously published procedures, are given. The synthesis of arbitrary switching circuits is treated as a linear programming problem, and a table of all four-variable circuits in which no circuit requires more than three cores is presented.

53. Muroga, S., Takasu, S. and Toda, I. Determination of the structure of a majority-decision element by the method of linear programming. JAPAN INST. ELECT. COMMUN. ENGRS. v. 43, n. 12, p. 1408–1, Dec 1960. (In Japanese)

A majority-decision element is one in which a finite number of inputs, having weights, are coupled with a single output, which is one or zero, decided by the majority decision which depends on the coupling numbers. The number of Boolean functions that can be realized by a single majority-decision element is rather small. The method of linear programming yields a criterion as to whether a given Boolean function can be realized or not by a single majority-decision element. The method also determines the most economical structure (coupling numbers and thresholds) of a majority-decision element realizing the function. A comprehensive list is given of majority-decision functions of 5 or less variables and of the structure of the majority-decision elements, determined by the linear programming method.

54. Muroga, Saburo Functional form of majority functions and a necessary and sufficient condition for their realizability. In AIEE PROC., SECOND SYMPOSIUM ON SWITCHING CIRCUITS, Detroit, Mich., 17–20 Oct 1961. p. 39–46.

"Majority functions" in this paper means "Boolean functions realizable with a single threshold device." The paper is divided into three parts. In part 3 a new NSCRM (Necessary and Sufficient Condition for the Realizability of Majority Functions) is presented. No one has yet been able to express the NSCRM purely in terms of Boolean equations. All NSCRM's, including that of this paper, as the author himself

states, may be regarded as restatements of Ky Fan's theorem on the consistency of simultaneous linear inequalities and all are expressed in (non-Boolean) linear algebraic terms. While NSCRM's of Chow and Elgot use all 2^n inequalities, each corresponding to each of all combinations of n inputs, the present NSCRM (Theorem 3.4, Proof is not given in the Symposium Proceedings) uses only those corresponding to prime implicants of the original function f and of the dual f^d. In a previous paper, the same author pointed out the equivalence of the NSCRM to a linear programming problem and showed a procedure based on the prime implicants which results in a considerable reduction of the number of inequalities and the number of arithmetic operations necessary for solving the linear programming problem. Thus, the present NSCRM may well be regarded as a restatement of his own results in a more closed mathematical form.

In part 2 it is shown that a majority function f and the dual f^d of n variables and the self-dual functions $xf + \bar{x}f^d$ of n + 1 variables are all majority functions and are characterized by the same n + 1 weights.

In parts 1 and 2, a class of Boolean functions satisfying some of the necessary but not sufficient conditions for majority functions is studied. Two functions are said to be comparable if one implies another. A function comparable to its own dual is called dual comparable. A function is called k-comparable if any two complimentary k constraints imposed on the variables give two comparable functions. "k-monotonicity" and "unateness" are respectively equivalent to up to k comparability and 1 (one) comparability. These classes of functions are helpful for clarifying the mutual relationships of various necessary conditions for the realizability of majority functions. Though no practical application is disclosed in this paper, the results will be applicable to synthesis and analysis of threshold logical circuits in the same manner as unateness and k-monotonicity have been.

In part 3 (theorem 3.3), it is shown that the sum of optimum weights of a positive self-dual majority function is always an odd integer provided that the optimum weights are all integers. The author and Elgot extended this into a conjecture that all majority functions would have this property, and stated it as an open problem at the same symposium. However, E. F. Moore has shown a majority function of 12 variables having non-integer optimum weights and a counterexample, of 14 variables, to the odd integer sum property has been constructed from Moore's function mentioned above. The open problem, therefore, is now known to be false.

55. Muroga, S.
The principle of majority decision logical elements and the complexity of their circuits.
In PROC. INTERNATL. CONF. ON INFORMATION PROCESSING, Paris, UNESCO, 1960, p. 400–407.

The logical element based on the majority decision principle, the binary value of the output of which depends on the majority of the input binary values, is defiend. A mathematical model is considered, as well as some fundamental properties of the function the element can represent and the complexity of the circuits involved. The consideration of the relative amplitudes of input couplings is important in that it permits the element to represent a number of symmetrical and asymmetrical functions, the forms of which are limited. Synthesis of a switching circuit by means of such elements is less complicated than by means of relays, as these elements can perform more complex logical operations. However, the number of inputs is limited by engineering difficulties. A unique feature of the element based on the majority decision principle is shown by the synthesis of a circuit representing a symmetrical function.

56. Muroga, S.
Restrictions in synthesis of a network with majority elements. IRE PROC. v. 49, n. 9, p. 1455, Sep 1961.

Refers to "input logic" theory in connection with digital computers. This is a note summarizing and discussing results obtained by a number of authors. Emphasis is placed on the problem of physical realizability of the network.

57. Muroga, S., Toda, I. and Takasu, S.
Theory of majority decision elements. J. FRANKLIN INST. v. 271, n. 5, p. 376–418, May 1961.

After some preliminary definitions, theorems are derived about some properties of the majority decision function and a necessary condition for its realizability by a single element; about the forms of functions realizable by a single majority decision element and upper and lower bounds to how many; about a criterion of realizability and the structure determination of the majority decision element for a given function by linear programming; and in order to check the properties derived a computer was used to find all majority decision functions of up to 6 variables and the structures of elements to realize these.

58. Myhill, J. and Kautz, W. H.
On the size of weights required for linear-input switching functions. IRE TRANSACTIONS ON ELECTRONIC COMPUTERS v. EC-10, n. 2, p. 288–90, Jun 1961.

Although only a small fraction of all switching functions are linear-input functions, it is known that an arbitrary combinational switching function can be realized in a network of such devices. If the nature of the device imposes any restriction on the maximum size of input weights, this will probably increase the number of such devices required for the realization of arbitrary switching functions.

59. Nagamori, K.
Parametron computer circuits. **ELECTRONICS** v. 33, p. 73–78, 3 Jun 1960.

After a discussion of the characteristics and coupling of parametrons, brief descriptions are given of circuits for: AND element; OR element; NOT element; shift register; half adder; full adder; serial adder; parallel adder; high-speed carry adder; multiplier; counter; reversible counter; code converter; and input-output translator.

60. Onyshkevych, L. S., Kosonocky, W. F. and Lo, A. W.
Parametric phase-locked oscillator – characteristics and applications to digital systems. **IRE TRANS. ELECTRONIC COMPUTERS** v. **EC-8**, n. 3, p. 277–86, Sep 1959.

The ability of the parametric phase-locked oscillator (p.l.o.) to detect, amplify, and store binary digital signals in the form of two distinct phases of a carrier, makes it possible to use the device as the sole component in a digital computer system. The variable-capacitance version operates readily at kilomegacycle frequencies, thus forming the basis of a digital computer at a kilomegacycle clock rate. The results of an investigation of the behavior and possible applications of the variable-capacitance p.l.o. are presented. The investigation was supported by experimental work with lumped-component variable-capacitance l.p.o's. at 5 Mc/s and microwave variable-capacitance p.l.o's. at 4 Mc/s. The steady-state behavior of the device is described; variations of the output voltage with pump voltage, loading, tuning and frequency variations are presented in the form of characteristic curves. Results indicate that the device is rather insensitive to reasonable changes in operating conditions and parameter values. The transient behavior of the p.l.o. shows that the device can be switched in a number of different ways. Five such modes of operation are discussed; these are phase initiation, forced switching, burst generation, tri-stable operation and unconditional switching. Each of these modes has particular advantages for various applications. Switching times of the order of 3 to 10 cycles of the signal frequency are readily obtainable. The various modes of operation of the device suggest a number of applications both in logic and in memory. To illustrate the versatility of the device, a random access memory is described as an example.

61. Paull, M. C. and McCluskey, E. J.
Boolean functions realizable with single threshold devices. IRE PROC. v. 48, p. 1335–1337, Jul 1960.

Letter discussing the properties of the Boolean functions which can be realized with a single threshold device, such as a magnetic core.

62. Pease, M. C.
ANALYTIC PROOF OF OPERABILITY OF A SECOND-ORDER NEURISTOR LINE. Stanford Research Inst., Menlo Park, Calif. Interim rept. no. 3, Feb 61, 45p. (Contract Nonr-32-200) ASTIA AD-253 333.

The equations for a particular type of Neuristor are studied and sufficient conditions developed for the existence of the type of solutions required. Mathematically, the problem is that of finding sufficient conditions on a non-linear equation of the Lienard type that will assure the existence of a limit-cycle solution. The term Neuristor, which is derived from neuron, describes a very general class of non-linear devices that exhibit some of the propagation properties of the nerve axon. Devices of this type can be used to transmit information without attenuation or distortion. The topologic relations of such devices which will permit their employment in logical structures has been worked out in some detail. While the existence of lines exhibiting Neuristor behavior is well established, no analytic proof of such a line, or rigorous statement of the necessary conditions for its existence in physically realizable terms, has been available. That certain lines should work has been inferred from physical arguments. Other lines have been computed or observed. But the line considered is the first for which analysis has given general conditions which are sufficient to assure Neuristor behavior. This work, therefore, is significant in demonstrating mathematical techniques which may ultimately prove to be of general importance to the study of Neuristors.

63. Pease, M. C.
ANALYTIC PROOF OF OPERABILITY OF A SECOND-ORDER NEURISTOR LINE. Stanford Research Inst., Menlo Park, Calif. Rept. for 23 June 60–30 June 61 on Molecular Electronics. Rept. no. ASD TN 61-40, Jun 61, 45p. (Contract AF 33(616)7567, Proj. 4159) ASTIA AD-263 631.

The equations for a particular type of Neuristor are studied and sufficient conditions developed for the existence of the type of solutions required. Mathematically, the problem is that of finding sufficient conditions on a non-linear equation of the Lienard type that will assure the existence of a limit-cycle solution. The term "Neuristor," which is derived from "neuron," describes a very general class of non-linear devices that exhibit some of the propagation properties of the nerve axon. Devices of this type can be used to transmit information without attenuation or distortion. The topologic relations of such devices which will permit their employment in logical structures has been worked out in some detail. The physical realizability of the general class is demonstrated, first by the neural axon itself, and second by various electronic lumped-element lines using, for example, relays or Esaki diodes, that have been built and shown to exhibit the requisite behavior.

64. Pierce, W. H.
Adaptive decision elements to improve the reliability of redundant systems. IRE INTERNATIONAL CONVENTION RECORD v. 10, n. 4, p. 124–131, 1962.

Summary and Conclusions

1. The optimum use of redundant computing circuits is attained by the insertion of decision elements which compute a statistical decision.
2. When errors are independent, a simple vote-taker can make the optimum decision from binary or analog inputs.
3. Adaption is necessary to implement the optimum decision, since the pertinent error probabilities will have to be measured. The adaption may be accurate or crude; many different adaption circuits may be used.
4. Analyses have established that the binary vote-taker can maintain its reliability by feeding back its own output to judge the reliability of its inputs, and that catastrophic failures can be detected in an analog vote taker by feeding back its own output.
5. Previous work dating back to von Neumann has established a pattern of using decision elements so as to tolerate errors in logic circuits, vote-takers, and interconnections.

65. Pierce, W. H.
IMPROVING RELIABILITY OF DIGITAL SYSTEMS BY REDUNDANCY AND ADAPTION. Stanford Electronics Labs., Stanford U., Calif. Technical rept. no. 1552-3 17 Jul 61, 121p. (Contract Nonr-22524, Proj. NR 373 360) ASTIA AD-261 113.

Redundancy and adaption will have engineering value in improving the reliability of digital systems if they can provide reliability not otherwise attainable, or if they can provide reliability more economically than other methods. The specific methods of using linearly separable decision elements proposed in this thesis show promise of value by both of the above criteria. Decision elements provide a means of overcoming the non-zero failure probability which will always be associated with every component of a digital system. They also permit systems with various amounts of component reliability to meet the same system reliability specifications by using appropriate amounts of redundancy and adaption. A given system reliability may be attained most economically by a redundancy greater than one. The examples calculated for system yield and lifetime show that the factor of increase in system yield or lifetime can be considerably more than the factor by which the redundancy is increased. The examples also indicate the possibility that the factor of increase in reliability of adaptive circuits over unadaptive ones could exceed the cost factor of the adaptive circuits.

66. Piske, Andreus August, Jr.
ASYNCHRONOUS DIGITAL LOGIC CIRCUITS USING NEURISTORS. Air Force Inst. of Tech., Wright-Patterson Air Force Base, Ohio.
(Master's thesis) Rept. no. GA/EE/61-3
Aug 61, 68p. ASTIA AD-269 418.

A study was made of the use of neuristors in the construction of asynchronous digital logic circuits. Specifically, the primary objective was the development of a formalized method for the design and the construction of asynchronous sequential circuits. The neuristor is an active device which acts as a one-dimensional channel along which a pulse may propagate at a constant velocity. Neuristors can be joined in 2 basic junction types: T and S junctions. A T-S junction is a combination of the 2 basic junction types. Using these 3 junction types, and, or and not circuits can be constructed. These basic circuits can be combined with a variable tree to construct any arbitrary combinational circuit. The neuristor has built-in delay. Sequential circuits can be analysed as delay devices and reduced to combinational circuits, which can be constructed using neuristors.

67. Pulvari, Charles F.
FERRIELECTRICS AS A POSSIBLE COMPUTER ELEMENT. Catholic U. of America, Washington, D. C. Rept. no. ASD TR 61-331, Oct 61, 34p.
(Contract AF 33(616)7423, Proj. 7062) ASTIA AD-269 542.

Research on high temperature ferroelectric storage media led to the discovery of a class of ferroelectric materials which require a minimum threshold field for switching. This property was heretofore not observed in ordinary ferroelectrics and compares with similar properties found in ferrite cores. Work was conducted essentially to exploit the phenomenon of ferroelectricity for application in computer logical devices. The feasibility of preparing capacitors having a ferroelectric as a dielectric was investigated. Limiting electrical parameters of the device were determined. Finally, a novel non-destructive readout method was investigated using electromagnetic interferometer techniques. With the experimental device constructed, the best signal-to-noise ratio obtained was 6:1. It is possible to obtain millions of readouts from a ferroelectric capacitor without destroying its state of polarization.

68. RCA Industrial Electronic Products, Camden, N. J.
PROJECT LIGHTNING. Final Rept. on Parametric Phase-Locked Oscillators. Special rept. no. 4-60 v. 1, 1 Sep 60. (Contract NObsr-77523) ASTIA AD-249 669.

An investigation was made of the problems associated with a high-speed carrier computer, and a computer subsystem was constructed employing sub-harmonic oscillators driven at 3.7 kmc. three-phase power source was modulated at a 30 mc rate so the interval between successive logic operations was 11 nanoseconds. The logic module is a balanced resonant varactor circuit having a pulsed subharmonic output at 1.85 kmc and a rise time of 3 nanoseconds. The output from each module, at a level of about 1 mw, is distributed through a network of resistors and coaxial lines to the modules of the following power supply phase. The logic is done at 1.85 kmc by forming a majority-of-three from the three inputs. This majority logic, with the readily available inversion operation, provides a universal set of logic gates. The subharmonic oscillator has advantages characteristic of a carrier computer, among these are the ability to transform impedance levels and the ability to get a logic inversion by adding a cable length which results in 180 degrees phase change of the signal. Advantages peculiar to the subharmonic oscillator system are the simplicity of the varactor and its inherently fast operation. This approach also has a high logic gain, and provides fully timed and amplitude limited pulses at the output of each module.

69. Reinecke, H., Jr.
CURRENT-OPERATED DIODE LOGIC GATES. Massachusetts Instit. of Tech. Lincoln Laboratory technical rept. no. 226, 21 Jul 1960, 43p.

The realization of switching functions using current-operated diode logic gates, which employ the direction of current as the binary variable, is presented. Two realization methods are discussed. The dual method consists of a set of rules which are analogous to the procedures employed for the realization of voltage-operated circuits. The lattice method is based on the transmission characteristics of a lattice network of four series-connected diodes. Either method is capable of realizaing any arbitrary transmission function, although the number of diodes required may be different. Hybrid networks, which combine the advantages of both methods, are described to illustrate the versatility of current-operated techniques. Practical design procedures are included to guide the designer in the application of the realization rules.

A static multiplier, capable of simultaneously multiplying two 4-bit binary numbers, was designed and built to demonstrate the practicability of current-operated diode logic gates. Approximately 270 diodes were required to construct the twenty gates used in the static multiplier. Dynamic tests of the assembled system indicated a reliable capability of 333,000 multiplications per second.

70. Remington Rand Univac Div., Sperry Rand Corp., St. Paul, Minn. PROJECT LIGHTNING. VOLUME I. Quarterly progress rept. no. 1, v. 1, 1 Jun–31 Aug 1960 on Phase 3. Rept. no. PX 1599-1, v. 1, 31 Aug 60, 24p. (Contract NObsr-77521) ASTIA AD-252 906.

An investigation was made to find the most reliable semiconductor devices for Lightning equipment. The design plans for the ultrahigh-speed memory (UHSM) were revised. The primary change is the use of larger-diameter film spots than previously planned. Transistors were tested to determine which came closest to fulfilling the requirements for use in memory circuits. The physical layout and mode of operation of the UHS memory were reviewed. A study was made of 4 basic logic packages. Progress was made on the development of a general block diagram. A study was mde of allowable propagation delays, pulse propagation characteristics, and the techniques for clock distribution in producing waveforms. An initial module-assembly study was made. Electron-beam welding was investigated. (Author)

71. Remington Rand Univac Div., Sperry Rand Corp., St. Paul, Minn. PROJECT LIGHTNING. VOLUME II. Quarterly progress rept. no. 1, v. 2, 1 Jun–31 Aug 60 on Phase 3. Rept. no. PX 1599-1, v. 2, 31 Aug 60, 48p. (Contract NObsr-77521) ASTIA AD-252 907.

Contents:

Film-core program
- Film-deposition techniques
- Apparatus and instrumentation
- Measurements
- Film-switching instrumentation
- Ferromagnetic resonance studies
- Applications

Mathematics and logic research
- Generalization by proof reappraisal
- Majority-logic analogs of Boolean generalized fundamental theorem

Polyadic generalization of axiom set

72. Remington Rand Univac Div., Sperry Rand Corp., St. Paul, Minn. PROJECT LIGHTNING. VOLUME II. Quarterly progress rept. no. 5, v. 2, 1 Jun–31 Aug 61 on Phase 3. Rept. no. PX 1599-5, v. 2, 31 Aug 61, 57p. (Contract NObsr-77521) ASTIA AD-273 749.

Contents:

Film-core program
- Film-deposition techniques
- Apparatus and instrumentation
- Film-property measurements
- Switching and resonance studies
- Applications

Mathematics and logic research
- Improved general-purpose logic array
- Majority-logic comparator
- Majority-minority conversion theorem

Lightning test machine
- High-speed memory stack design
- Sense amplifier
- High-level word translation
- Film strips
- Reproducibility of electroplated thin films

73. Ross, William Carroll
NEURISTOR CIRCUITS TO ACCOMPLISH SOME DIGITAL COMPUTER OPERATIONS. Air Force Inst. of Tech., Wright-Patterson Air Force Base, Ohio. (Master's thesis) Rept. no. GA/EE61-4 Aug 61, 33p. ASTIA AD-268 972.

Digital computer circuits were constructed using neuristors. A neuristor is a one-dimensional channel along which pulses may propagate, the pulses taking the form of propagating discharges having the following properties: threshold stimulability, attenuationless propagation, uniform velocity of propagation, and refractive period following the passage of a discharge past any point of a channel. Two neuristor pulse sequences representing binary numbers are fed simultaneously into a neuristor add circuit; a pulse sequence emerges which represents the sum of the two pulse sequences. Similar circuits are developed for subtraction, multiplication, division and other elementary operations.

74. Sarrafian, G. P.
Tunnel diode threshold logic. IRE INTERNAT. CONVENTION RECORD v. 9, n. 2, p. 271–6, 1961.

Advantages of the tunnel diode as a computer element are high speed, low power dissipation and potentially low cost. The d.c. characteristics of the device make it highly suitable for use in threshold logic where many complex logic functions of a number of variables can be performed by a single element, thereby reducing the number of elements required. Some practical tunnel diode circuits which operate as threshold logic elements are shown. Design considerations are discussed, involving the effects of initial restrictions specified such as maximum fan-in and fan-out, component and power supply tolerances and maximum signal propagation time permitted.

75. Schauer, R. F., et al.
Some applications of magnetic film parametrons as logical devices. IRE TRANS. ON ELECTRONIC COMPUTERS v. EC-9, p. 315–320, Sep 1960.

High-frequency magnetic film parametrons which exhibit two- or three-state operation for a single bias condition are described. As a two-stable-state device, the magnetic film parametron can be used as a majority decision element in much the same way as the ferrite core parametron. Another useful logical two-stage device is a threshold element, in which the input excitation must reach a minimum level to sustain

oscillations. The magnetic film inductor, when suitably clocked, can be used as a gate to permit unilateral flow of information in a system. The gating action, controlled by the bias field, can result from the rectified output of a parametron. Proposed logical designs for a two-element binary adder, a binary shift counter, and a shift register are presented. The possibilities of three-state operation are also explored in the logical design of a seven-element ternary full adder.

76. Short, R. A.
A THEORY OF RELATIONS BETWEEN SEQUENTIAL AND COMBINATIONAL REALIZATIONS OF SWITCHING FUNCTIONS. Stanford University. 12 Dec 1960, 119p. ASTIA AD-253 137.

It is postulated that a useful theory of relations can be established between important classes of combinational and sequential digital networks. Such a theory could be useful in describing basic digital processes and in illuminating the essential differences between the two kinds of physical realisations of switching functions. The basic objectives are formalisation of these relations and development of procedures for transforming readily from one kind of network to another. By means of an abstract binary decision element, a particular kind of directed graph is defined that can be variously interpreted as a transfer contact network, a binary-decision program, or a particular kind of state diagram. These correspondences, plus certain functional assumptions, imply a set of rules governing permissible graph interconnections. Further restrictive assumptions extend the correspondences to include iterative combinational networks and conventional state diagrams. Transformation procedures between graphs with different interconnection rules and different minimisation criteria are developed.

77. Simon, H. A.
Modeling human mental processes. WJCC PROC. v. 19, p. 111–119, May 1961.

Several areas relating to the field of artificial intelligence are discussed. These are: 1) simulation of adaptive processes and goal seeking; 2) pattern recognition; 3) neural net simulation; and 4) symbol manipulation, concept formation and problem-solving behavior. Some of the epistemological difficulties in formulating nonquantitative mathematical theories are described, and the impact of computer-oriented research on the field is discussed. Several heuristic programming projects including the General Problem Solver are also described. It is pointed out that the largest gap in artificial intelligence research lies in the area of long-term memory processes.

78. Sims, D.
THE PARAMETRON USED AS A MAJORITY GATE FOR IMPROVING DIGITAL SYSTEM RELIABILITY.
Hermes Electronics Co. 1960, 19p. ASTIA AD-244 488.

A number of simple logical circuits are presented to illustrate logical design principles with parametrons. Using the basic design concepts of the parametron logic element, majority logic is applied to a full parallel adder. The majority logic adder was tested under a number of simulated failure conditions in which one-third of the majority gate elements were inactive. The adder operated under such failures as shorted inputs, shorted outputs, and open output windings.

79. Sims, R. C.
A survey of tunnel-diode digital techniques. IRE PROC. v. 49, p. 136–146, Jan 1961.

This paper is concerned with the use of the tunnel diode in memory and logic circuitry and discusses the major techniques that have been reported together with some that have been developed by the authors and others at the Bendix Research Laboratories. After briefly considering the major characteristics of tunnel diodes, various memory circuits are described with particular attention to random access matrices. The principles of tunnel diode logic design are illustrated by means of basic threshold circuits and OR, AND, NOT and other logic circuits are described.

80. Singleton, Richard C.
A TEST FOR LINEAR SEPARABILITY AS APPLIED TO SELF-ORGANIZING MACHINES. Stanford Research Inst., Menlo Park, Calif. May 62, 29p. (Contract Nonr-343800) AD-277 948.

Presented at the Conference on Self-Organizing Systems, held May 22–24, 1962, Chicago, Ill.

Threshold logic elements are widely used in self-organizing machines, as a means of separating binary patterns into two categories. The question of whether or not two given sets of binary patterns can be separated with a single threshold logic element is of considerable interest, since training by weight adjustment can succeed only for those sets of patterns which are separable. In investigating this problem, it is convenient to consider the binary patterns as vertices of the unit n-cube. If an (n - 1)-dimensional hyperplane can be passed through the cube in such a way that the two sets of vertices lie on opposite sides of the plane, the two sets are said to be linearly separable. The corresponding two sets of binary patterns can then, and only then, be

distinguished by a single threshold logic element. This report presents a new test for linear separability. The two sets of binary patterns are combined in a matrix, and a sequence of reductions applied to this matrix to obtain a smaller matrix to be solved as a linear programming or game problem.

81. Smay, T. A. and Pohm, A. V.
Design of logic circuits using thin films and tunnel diodes. **ELECTRONICS** v. 34, p. 59–61, Sep 1961.

Logic circuits using thin ferromagnetic films and tunnel diodes are discussed. Because of its negative resistance characteristic, the tunnel diode can be biased to operate at two stable voltage levels for a given current condition, while the single-domain ferromagnetic film has two stable magnetization orientations in the absence of external fields. Two types of toggling circuits are presented including schematics, characteristic curves, switching waveforms, and a theoretical discussion of operating principles. Both the tunnel diode and the thin ferromagnetic film operate at low voltage and moderate current levels and have high switching speeds. The primary difficulty in using such devices at present is the amount of amplification required to bring the sense winding signal up to a usable level. Improved deposition of films may result in greater energy transfer.

82. Stram, O. B.
Arbitrary Boolean functions of N variables realizable in terms of threshold devices. **IRE** PROC. v. 49, p. 210–220, Jan 1961.

A method for the logical design of single-stage, combinatorial switching circuits of n variables is presented. This method is applicable to circuits composed of threshold devices, such as magnetic cores, transistors with Kirchhoff adder inputs, parametrons, etc. A study of the constraints imposed by the form of the input portions of the threshold devices leads to the definition of certain classes of functions which are physically realizable in a single device. By the use of this method, arbitrary switching functions of as many as seven variables have been easily designed by hand computations.

83. Stram, O., Einhorn, S. and Celia, J.
MAGNETIC LOGICAL TRANSDUCERS.
Burroughs Corp. Aug 1961, 92p. ASTIA AD-268045.

A method is presented for the logical design of single-stage, combinatorial switching circuits of n-variables. It is applicable to circuits composed of threshold devices, such as magnetic cores, transistors with Kirchoff adder inputs, parametrons, etc. A study of the constraints imposed by the form of the input portions of the threshold devices leads to the definition of certain classes of functions, physically realisable in a single device. With this method, arbitrary switching functions of as many as seven variables were easily designed by hand computation. An algorithm for mechanising Boolean switching functions, by means of a net of magnetic toroidal cores, is described. The algorithm is referred to as Simplex which, in this application, is programmed for a digital computer. Computer-derived solutions specify the wiring configuration for a core or net of cores yielding a device for performing combinatorial logic. Switching functions are realizable in essentially one clock time.

84. Sutherland, C. W.
Limitations of the AND-OR to majority-logic conversion technique. IRE PROC. v. 49, p. 519, Feb 1961.

Letter referring to "A new concept in computing," R. Lindaman, ibid, v. 48, p. 257, Feb 1960, and demonstrating that the method there described for converting logical networks containing AND and OR functions to networks containing only majority decision elements is applicable to only 10 of the 256 possible switching functions of three variables.

85. Takahashi, H. and Goto, E.
Application of error-correcting codes to multi-way switching. In PROC. INTERNATL. CONF. ON INFORMATION PROCESSING. Paris, France, 15–20 Jun 1959. Paris, UNESCO, 1959, p. 396–400.

This paper describes a switching circuit for selecting one of a number of outputs. It uses a linear network of transformers to couple the drivers to threshold elements, and the connections are determined according to an error-correcting code. The application to the selection circuits of a parametron memory, in operation since May, 1958 is briefly described.

The principles are the same for this circuit as for the "load-sharing switching matrix" found independently at about the same time by Constantine. There are several contrasts in viewpoint. Takahashi and Goto use the outputs of the matrix to switch the memory devices directly, whereas Constantine uses the matrix to switch driver cores which in turn drive the X and Y lines on a core memory plane. With Constantine's choice of error-correcting code, the number of drivers required is the same as the number of outputs, so that as it is applied to the core memory, there is no reduction

in the number of drivers. The advantage lies in a great reduction in current required from each driver. Takahashi and Goto describe choices of codes which result in a significant reduction in the number of drivers. For example, a 2048 core memory could be addressed using the Golay code with 24 drivers and a selection ratio 3:1. (A conventional 32 × 64 coincident current plane would have 96 drivers and only a 2:1 selection ratio.) Furthermore, there would be reduction of driver current by a factor of 12, though Takahashi and Goto did not emphasize this advantage. Finally, Takahashi and Goto emphasize that the matrix will still select properly, with a reduced selection ratio, in spite of a limited number of driver failures, and indeed they found that their parametron memory would operate reliably with one driver failure and would have only intermittent errors with two driver failures.

86. Tanaka, R. I., et al
THRESHOLD SWITCHING TECHNIQUES.
Lockheed Aircraft Corp., Sunnyvale, Calif.
Interim engineering rept. no. 1, 20 Mar–20 Jun 61. Rept. no. 2-01-61-1. (Contract AF 33(616)8035). ASTIA AD-263 825.

The results are presented of approximately 3 months of work on a study of threshold switching techniques. A description is included of some analytic representations usable for describing the characteristics of a threshold switching element. Some aspects of a synthesis technique are described which are applicable to describing and testing linearly separable functions. Information is also included concerning a synthesis approach for designing a network consisting of a two-layered network of threshold elements where the elements have minimal weights and thresholds.

87. Tanaka, R. I., et al
THRESHOLD SWITCHING TECHNIQUES.
Lockheed Aircraft Corp., Sunnyvale, Calif.
Interim engineering rept. no. 2, July–Aug 61. Rept. no. 2-01-61-2, Aug 61, 78p. (Contract AF 33(616)8035) ASTIA AD-263 824.

The study continues to emphasize the derivation of synthesis techniques applicable to the design of switching networks which incorporate threshold devices. Significant progress on establishing feasibility and in deriving supporting mathematical proofs for some of the synthesis algorithms has been made. However, a second objective, related to the practical implementation of threshold switching networks, now supplements the original emphasis. Preliminary work on two topics is described which touch directly upon hardware implementation. These are: (1) The derivation of techniques for transforming a network of given threshold elements to another network whose elements each have a different number of inputs; and (2) A definition of the characteristics of threshold elements to determine the allowable limits on various parameters.

88. Tancrell, Roger H.
Impulse selection for core logic. J. OF APPLIED PHYSICS, SUPP., 32:40S-41S, Mar 61.

Impulse selection is a scheme for operating ferrite cores which have low values of coercive force. Two different threshold properties of a core are utilized. One threshold is the dc coercive force, which can be changed electrically. The other threshold results from the inertial magnetic effects within the core which are predominant when pulses of very narrow widths are applied. The switching behavior of ferrite cores is discussed when two threshold currents, a low amplitude current and an impulse of current, are combined. The application of this property to core logic is considered.

89. Toda, I., Kondo, M. and Muroga, S.
Majority decision functions of six variables.
JAPAN. REV. ELECT. COMMUN. LAB. v. 9, n. 5-6, p. 253-78, May-Jun 1961.

A method of obtaining all majority decision functions is described. A majority decision function is a logical function which can be represented by a single majority decision element, such as a parametron or magnetic core. It is shown that, given a majority decision function, its canonical representative can be easily determined from the intrinsic properties of such functions. Thus a set of possible candidates can be obtained for the canonical representatives, containing all the true representatives which can be separated by a method of linear programming. The proposed method is shown to be quite efficient compared with the conventional method. A table of all majority decision functions of six variables is shown, together with their optimum structures, and several properties of majority functions which were deduced from the table are given.

90. Tomlinson, T. B.
Switching circuits using bi-directional non-linear impedances. J. BRIT. INSTN. RADIO ENGRS. v. 19, n. 9, p. 571-91, Sep 1959.

In a brief general review of logic circuitry, a case is developed for a bi-directional, non-linear switching element. In order to compare circuits using such elements with those using standard semi-conductor diodes, the main features of diode gates are considered. Particular attention is paid to design of p-n-p transistor driver stages and their dependence on the logic sequence. Circuits using a bidirectional "constant voltage" element are described, using a "two-decision" AND gate. Possible types of constant voltage element are discussed and experimental results are given for multi-electrode silicon carbide devices. An interesting feature of the latter is the non-linear behavior of capacitance. An attempt is made to compare gating circuits employing constant voltage, bi-directional elements with standard diode gates from a performance/cost point of view. A "majority-logic" gate is made possible by a "constant current,"

bidirectional element. If one input is used as a control, this gate can become a many function gate, thus a 3-input gate can be controlled to act as a 3-AND, an OR, or a "2 or more out of 3" logical unit without change of input or output connections. Some possible realizations of the constant current device are discussed. A binary-octal decoder circuit and a simple binary full adder circuit are given as examples of the application of the non-linear elements and to illustrate their unusual features.

91. Wasserman, R.
DEVELOPMENT OF A MAJORITY GATE FOR IMPROVING DIGITAL SYSTEM RELIABILITY.
Hermes Electronics Co., Cambridge, Mass.
Rept. no. M-809, 2 Nov 1959, 51p. (Contract Nonr-2133(00)) ASTIA AD-229 364.

Logical design procedure for the efficient use of redundancy in improving the reliability of digital systems is discussed. This calls for the development of a highly reliable, simply constructed, majority gate. Requirements and design considerations for the majority gate using magnetic cores as logical building blocks are presented. Logical design principles for a shift register, dynamic flip-flop, logical gate functions, binary counter, comparator, and two-input full adder are also considered. A 6-core majority gate module and a 9-core majority gate module are discussed.

91a. Willis, David G.
Minimum weights for threshold switches. Paper presented at a SYMPOSIUM ON THE APPLICATION OF SWITCHING THEORY IN SPACE TECHNOLOGY, SUNNYVALE, CALIF., FEB 27 AND 28 AND 1 MAR 1962. PROCEEDINGS to be published by Stanford University Press, 1963.

After defining threshold functions, the author admits that his definition, in common with most definitions of threshold functions, does not provide any simple means of telling whether a given switching function is or is not a threshold function. Two theorems are offered which provide a test for determining whether a given set of weights is minimum or uniquely minimum. Because the tests are formulated in terms of linear equations they are considerably simpler than the usual methods of manipulating inequalities.

92. Winder, R. O.
MORE ABOUT THRESHOLD LOGIC. David Sarnoff Research Center, Princeton, N. J. Scientific rept. no. 1. Rept. no. AFCRL-701, 14 Jul 61, 13p. (Contract AF 19(604)8423) ASTIA AD-264 049.

Ideas are discussed on Switching Theory and Logical Design. The main subject is compound synthesis. The family of functions of n arguments realizable in a single stage becomes a vanishing fraction of all switching functions of n arguments as n grows (for n equals 7 the ratio is about 10 to the 28-1/2 power). An algorithm is provided for determining 2-realizability – realizability with two threshold elements. The approach produces a good solution in any case, but one guaranteed optimal only for 2-realizable functions. A geometric terminology is used; this new language is also used where higher necessary conditions for realizability are discussed. A conjecture that certain of these conditions might be sufficient is disproved; three related conditions are treated in a common language. Optimal integral single-stage realizations are considered. A conjecture, that such a realization gives equal arguments equal weights, is disproved.

93. Wray, W. J., Jr.
D. C. design of resistance-coupled transistor logic circuits. I. R. E. TRANS. CIRCUIT THEORY v. CT-6, n. 3, p. 304–10, Sep 1959.

Worst-case d.c. design equations for resistance-coupled transistor logic circuits are presented and discussed. A solution is chosen in a form which provides for setting switching transient times in advance of calculating the d.c. design. All constants are discussed and the algebraic solution is obtained for values of the unknown resistors and voltages. A numerical example illustrates a typical design with five inputs and five outputs, using the type GT-759 transistor.

94. Wray, W. J., Jr.
Worst case design of variable-threshold TRL circuits. IRE TRANSACTIONS ON ELECTRONIC COMPUTERS v. EC-11, p. 382–390, Jun 1962.

Summary – Now that standard Transistor Resistor Logic is well understood and widely used, the possibilities for reducing component count by changing the height of the switching threshold, as measured in units of input, are being explored. This paper presents the worst case design formulation, both steady-state and transient, for such

variable-threshold circuitry. In addition there is a brief discussion of the logic represented. Numerical results illustrate the logical possibilities and the effect of increasing the threshold on transient behavior.

95. Yochelson, S. B.
Diodeless core logic circuits. IRE WESCON CONVN. RECORD n. 4, p. 82–95, 1960.

This paper is concerned with a system of logic circuitry, developed at Goodyear Aircraft Corporation, which is based on the use of conventional square-loop ferrite magnetic cores for all operations, semiconductor or other active coupling elements not being required. It differs from other diodeless core logic systems in that there are no inherent limits on speed, logic capabilities or branching (fan out) capabilities other than the characteristics of the cores themselves. The system uses the threshold characteristics of the magnetic cores as the nonlinearity needed to achieve directivity of information flow. In addition to the cores needed as information storage elements, added cores are used in place of the diodes or similar nonlinear devices found in conventional core logic systems. Control of directivity is achieved by biasing certain cores up to their thresholds, resulting in the inhibiting of some cores from switching and the aiding of the switching of others. Arrangements are made so that the voltages induced into each coupling loop by a switching core are always opposed by another switching core. Hence, there is no need to reset some cores slowly.

SUBJECT INDEX